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22423 Linear Integrated Circuit MCQ Questions and Answers

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Linear Integrated Circuit Questions and Answers

1. Which is not the internal circuit of operational amplifier?

a) Differential amplifier

b) Level translator

c) Output driver

d) Clamper

Answer: d

Explanation: Clamper is an external circuit connected at the output of Operational amplifier, which clamp the output to desire DC level.

2. The purpose of level shifter in Op-amp internal circuit is to

a) Adjust DC voltage

b) Increase impedance

c) Provide high gain

d) Decrease input resistance

Answer: a

Explanation: The gain stages in Op-amp are direct coupled. So, level shifter is used for adjustment of DC level.

3. How a symmetrical swing is obtained at the output of Op-amp

a) Providing amplifier with negative supply voltage

b) Providing amplifier with positive voltage

c) Providing amplifier with positive& negative voltage

d) None of the mentioned

Answer: c

Explanation: For example, consider a single voltage supply +15v. During positive half cycle the output will be +5v and -10v during negative half cycle.

Therefore, the maximum peak to peak output swing, -5v (-10v) = -15v (Asymmetrical swing).

So, to get symmetrical swing both positive and negative supply voltage with bias point fixed suitably is required.

4. What is the purpose of differential amplifier stage in internal circuit of Op-amp?

a) Low gain to differential mode signal

b) Cancel difference mode signal

c) Low gain to common mode signal

d) Cancel common mode signal

Answer: d

Explanation: Any undesired noise, common to both of the input terminal is suppressed by differential amplifier.

5. Which of the following is not preferred for input stage of Op-amp?

a) Dual Input Balanced Output

b) Differential Input Single ended Output

c) Cascaded DC amplifier

d) Single Input Differential Output

Answer: c

Explanation: Cascaded DC amplifier suffers from major problem of drift of the operating point, due to temperature dependency of the transistor.

6. What will be the emitter current in a differential amplifier, where both the transistor are biased and matched? (Assume current to be IQ)

a) IE = IQ/2

b) IE = IQ

c) IE = (IQ)2/2

d) IE = (IQ)2

Answer: a

Explanation: Due to symmetry of differential amplifier circuit, current IQ divides equally through both transistors.

7. From the circuit, determine the output voltage (Assume αF=1)

a) VO1=3.9v , VO2=12v

b) VO1=12v , VO2=3.9v

c) VO1=12v , VO2=0v

d) VO1=3.9v , VO2=-3.9v

Answer: b

Explanation: The voltage at the common emitter 'E' will be -0.7v, which make Q1 off and the entire current will flow through Q2.

⇒ VO1 = VCC VO2= VCC-αF×IQ×RC,

⇒ VO1 = 12v , VO2=12v-1×3mA×2.7k = 3.9v.

8. At what condition differential amplifier function as a switch

a) $4VT < Vd < -4VT$

b) $-2VT \leq Vd \leq 2VT$

c) $0 \leq Vd < -4VT$

d) $0 \leq Vd \leq 2VT$

Answer: a

Explanation: For Vd > 4VT, the output voltage are VO1 = VCC, VO2= VCC-αF IQRC. Therefore, a transistor Q1 will be ON and Q2 will be OFF. Similarly for Vd> -4VT, both transistors Q2 & Q1 will be ON.

9. For Vd > ±4VT, the function of differential amplifier will be

a) Switch

b) Limiter

c) Automatic gain control

d) Linear Amplifier

Answer: b

Explanation: At this condition, input voltage of the amplifier is greater than ±100mv and thus acts as a limiter

10. Change in value of common mode input signal in differential pair amplifier make

a) Change in voltage across collector

b) Slight change in collector voltage

c) Collector voltage decreases to zero

d) None of the mentioned

Answer: a

Explanation: In differential amplifier due to symmetry, both transistors are biased and matched. Therefore, Voltage at each collector will be same.

11. Find collector current IC2, given input voltages are V1=2.078v & V2=2.06v and total current IQ=2.4mA. (Assume α=1)

a) 0.8mA

b) 1.6mA

c) 0.08mA

d) 0.16mA

Answer: a

Explanation: Collector current, IC2=αF×IQ/(1+eVd⁄VT),

VT = Volts equivalent of temperature = 25mv,

⇒ Vd = V1-V2 =2.078v-2.06v=0.018v (equ1)

Substituting equation 1,

⇒ Vd/VT = 0.018v/25mv = 0.72v (equ2)

Substituting equation 2,

⇒ IC2= 1×2.4mA/(1+e0.72) = 2.4mA/(1+2.05) = 0.8mA.

12. A differential amplifier has a transistor with β0= 100, is biased at ICQ = 0.48mA. Determine the value of CMRR and ACM, if RE =7.89kΩ and RC = 5kΩ.

a) 49.54 db

b) 49.65 d

c) 49.77 db

d) 49.60 db

Answer: b

Explanation: Differential mode gain, ADM= -gmRC and Common mode gain,

⇒ ACM= -(gmRC)/(1+2gmRE)

(for ß0≫1).

Substituting the values,

⇒ gm= ICQ/VT = 0.48mA/25mv=19.2×10-3Ω-1

⇒ ADM= -gm×RC= -19.2×10-3Ω-1×5kΩ= -96

⇒ ACM= -(gmRC)/(1+2gmRE)= -(19.2×10-3Ω-1×5kΩ) /(1+2×-⇒ 19.2×10-3Ω-1×7.89kΩ) = -0.3158

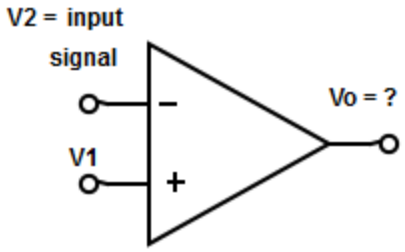
CMRR = -96/-0.3158= 303.976

=20log303.976

=49.65db

This set of Linear Integrated Circuit Multiple Choice Questions & Answers (MCQs) focuses on "Ideal Operational Amplifier".

13. Determine the output from the following circuit



a) 180o in phase with input signal

b) 180o out of phase with input signal

c) Same as that of input signal

d) Output signal cannot be determined

Answer: b

Explanation: The input signal is given to the inverting input terminal. Therefore, the output Vo is 180o out of phase with input signal V2.

14. Which of the following electrical characteristics is not exhibited by an ideal op-amp?

a) Infinite voltage gain

b) Infinite bandwidth

c) Infinite output resistance

d) Infinite slew rate

Answer: c

Explanation: An ideal op-amp exhibits zero output resistance so that output can drive an infinite number of other devices.

15. An ideal op-amp requires infinite bandwidth because

a) Signals can be amplified without attenuation

b) Output common-mode noise voltage is zero

c) Output voltage occurs simultaneously with input voltage changes

d) Output can drive infinite number of device

Answer: a

Explanation: An ideal op-amp has infinite bandwidth. Therefore, any frequency signal from 0 to ∞ Hz can be amplified without attenuation.

16. Ideal op-amp has infinite voltage gain because

a) To control the output voltage

b) To obtain finite output voltage

c) To receive zero noise output voltage

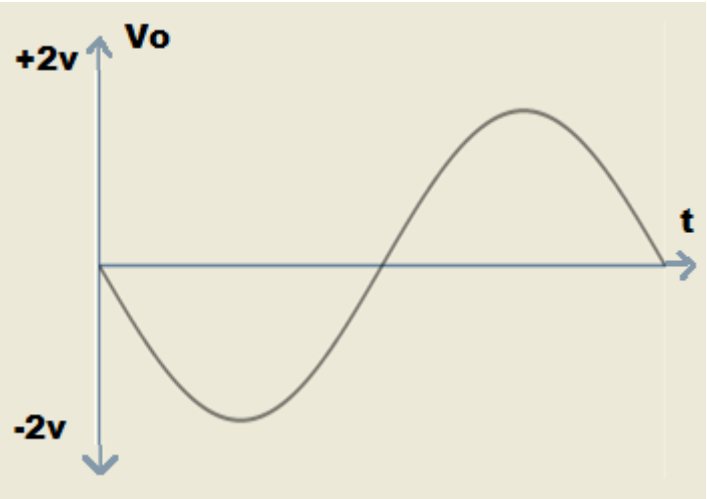
d) None of the mentioned

Answer: b

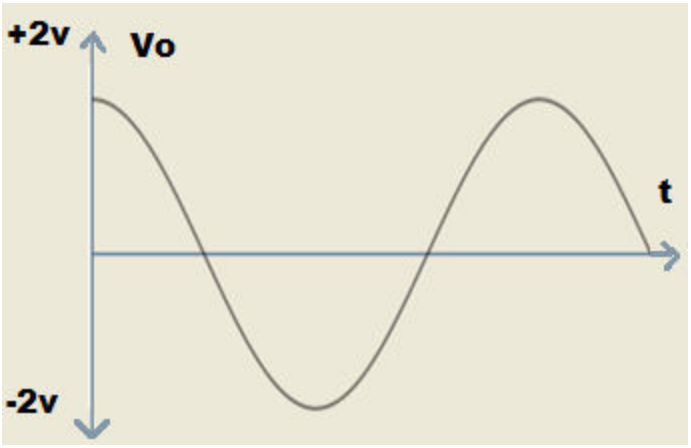
Explanation: As the voltage gain is infinite, the voltage between the inverting and non-inverting terminal (i.e. differential input voltage) is essentially zero for finite output voltage.

17. Determine the output voltage from the following circuit diagram?

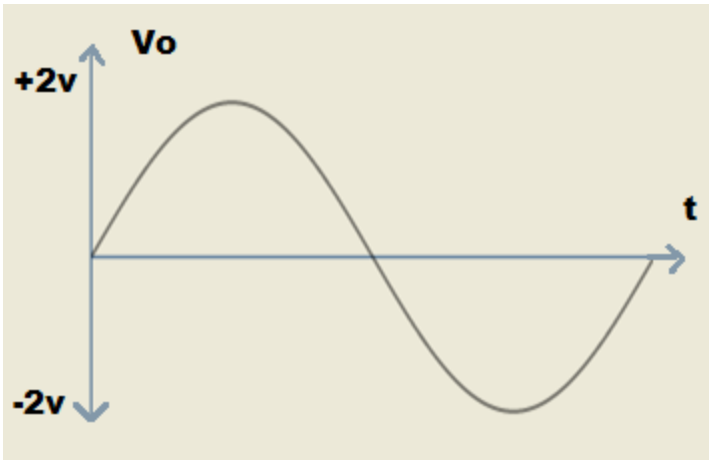
(a)



(b)



(c)



d) None of the mentioned

Answer: c

Explanation: In an ideal op-amp when the inverting terminal is zero. The output will be in-phase with the input signal.

18. Find the output voltage of an ideal op-amp. If V1 and V2 are the two input voltages

a) VO= V1-V2

b) VO= A×(V1-V2)

c) VO= A×(V1+V2)

d) VO= V1×V2

Answer: b

Explanation: The output voltage of an ideal op-amp is the product of gain and algebraic difference between the two input voltages.

19. How will be the output voltage obtained for an ideal op-amp?

a) Amplifies the difference between the two input voltages

b) Amplifies individual voltages input voltages

c) Amplifies products of two input voltage

d) None of the mentioned

Answer: a

Explanation: Op-amp amplifies the difference between two input voltages and the polarity of the output voltage depends on the polarity of the difference voltage.

20. Which is not the ideal characteristic of an op-amp?

a) Input Resistance –> 0

b) Output impedance –> 0

c) Bandwidth –> ∞

d) Open loop voltage gain –> ∞

Answer: a

Explanation: Input resistance is infinite so almost any signal source can drive it and there is no loading of the preceding stage.

21. Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)

a) 8v

b) 4v

c) -4v

d) -2v

Answer: d

Explanation: The output voltage, VO = (Vin1– Vin2)

=> 12v=3×(2- Vin2)

=> Vin2= -2v.

22. Which factor determine the output voltage of an op-amp?

a) Positive saturation

b) Negative saturation

c) Both positive and negative saturation voltage

d) Supply voltage

Answer: c

Explanation: Output voltage is proportional to input voltage only until it reaches the saturation voltage. The output cannot exceed the positive and negative saturation voltage. These saturation voltages are specified by an output voltage swing rating of the op-amp for given values of supply voltage.

23. What is the level of the output voltage of a ladder-network conversion?

A. The analog output voltage proportional to the digital input voltage

B. The digital output voltage proportional to the linear input voltage

C. A fixed digital value V_{ref}

D. A fixed analog value V_{ref}

Answer: Option A

24. Which of the following is not a linear/digital IC?

A. Phase-locked loop

B. Voltage-controlled oscillator

C. Passive filter

D. Comparator

Answer: Option C

25. A 339 IC is an example of a fourteen-pin DIP that can be made to function as a _____.

A. comparator

B. 555 timer

C. D to A converter

D. ladder network

Answer: Option A

26. What is the minimum number of conversions per second of a clock rate of 1 MHz operating a 10-stage counter in an ADC?

A. 1000 B. 976

C. 769 D. 697

Answer: Option B

27. Which of the following is (are) the results of improvements built into a comparator IC?

A. Faster switching between the two output levels

B. Noise immunity

C. Outputs capable of directly driving a variety of loads

D. All of the above

Answer: Option D

28. What is the first phase of the dual-slope method of conversion?

A. Connecting the analog voltage to the integrator for a fixed time

B. Setting the counter to zero

C. Connecting the integrator to a reference voltage

D. All of the above

Answer: Option A

29. What is the maximum conversion time of a clock rate of 1 MHz operating a 10-stage counter in an ADC?

A. 1.024 s

B. 102.3 ms

C. 10.24 ms

D. 1.024 ms

Answer: Option D

30. On which of the following does the conversion depend in ladder-network conversion?

A. Comparator

B. Control logic

C. Digital counter

D. Clock

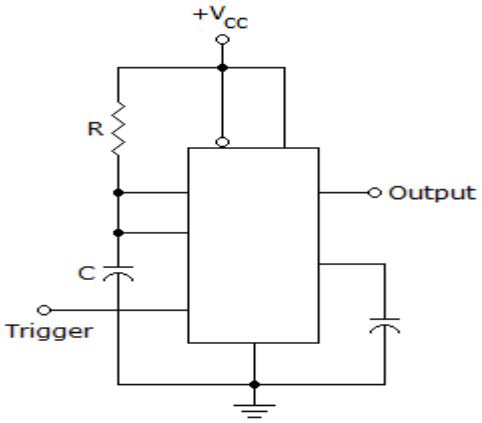
Answer: Option A

31. The voltage-controlled oscillator is a subset of the "test bench" function generator.

A. True B. False

Answer: Option A

32. Which application best describes this 555 timer circuit?



A. Monostable multivibrator

B. Astable multivibrator

C. Bistable multivibrator

D. Free-running multivibrator

Answer: Option A

33. Which of the following applications include a phase-locked loop (PLL) circuit?

A. Modems

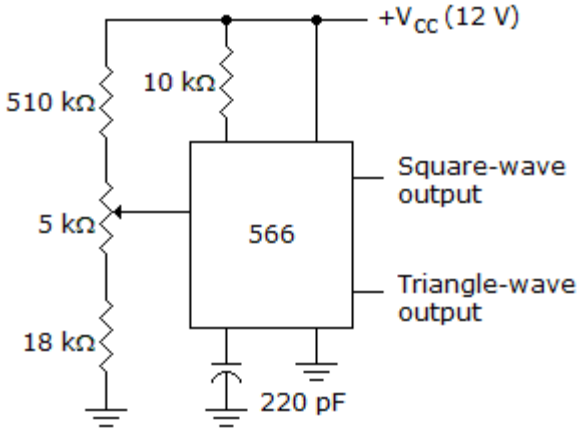
B. Am decoders

C. Tracking filters

D. All of the above

Answer: Option D

34.Determine the free-running frequency when R3 is set to 2.5 k



A. 19.7 kHz

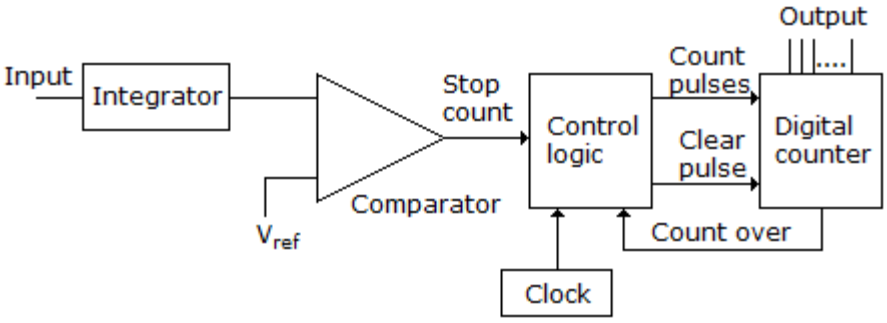
B. 32.5 kHz

C. 116.39 kHz

D. 212.9 kHz

Answer: Option C

35. This figure is a block diagram of a(n) _____.



A. ADC

B. DAC

C. comparator

D. 555 timer

Answer: Option A

36. What is the function of a ladder network?

A. Changing an analog signal to a digital signal

B. Changing a linear signal to a digital signal

C. Changing a digital signal to an analog signal

D. None of the above

Answer: Option C

37. Which of the slope intervals of the integrator does the counter in the analog-to-digital converter (ADC) operate?

A. Positive

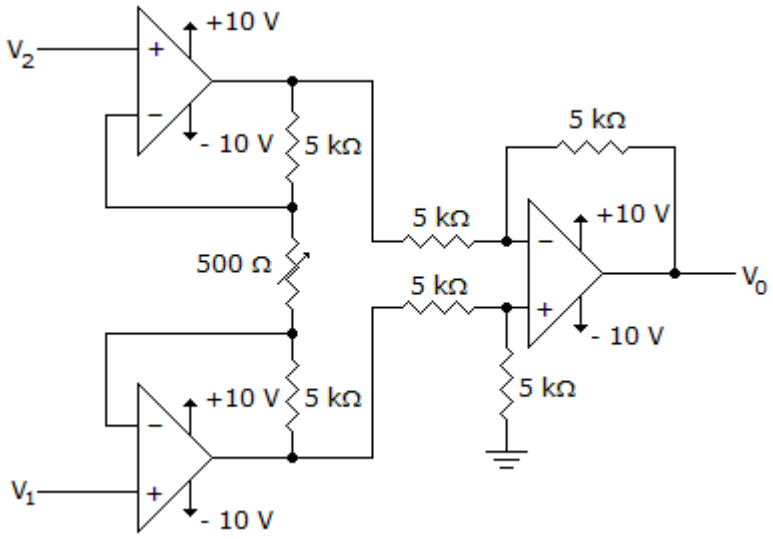
B. Negative

C. Both positive and negative

D. Neither positive nor negative

Answer: Option C

38. Calculate the output voltage for this circuit when V1 = 2.5 V and V2 = 2.25 V.



A. –5.25 V

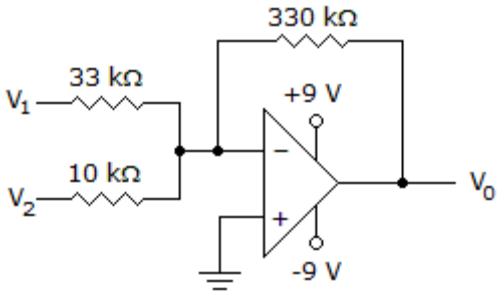
B. 2.5 V

C. 2.25 V

D. 5.25 V

Answer: Option D

39.Calculate the output voltage if V1 = –0.2 V and V2 = 0 V.



A. 0 V

B. –6.6 V

C. –4 V

D. 2 V

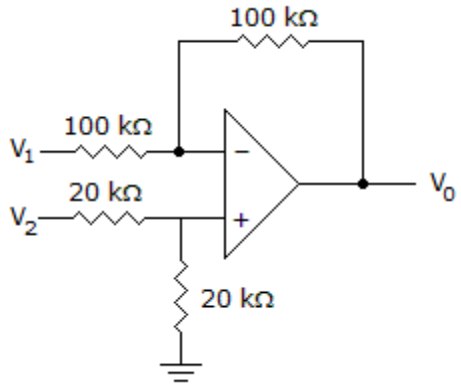
Answer: Option D

40. A number of op-amp stages can be used to provide separate gains.

A. True B. False

Answer: Option A

41. Determine the output voltage when $V_1 = -V_2 = 1$ V.



A. 0 V

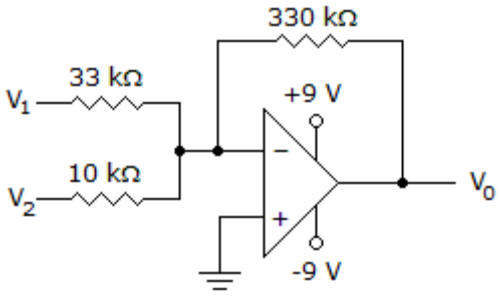
B. –2 V

C. 1 V

D. 2 V

Answer: Option B

42. Calculate the output voltage if V1 = V2 = 0.15 V.



A. 0 V

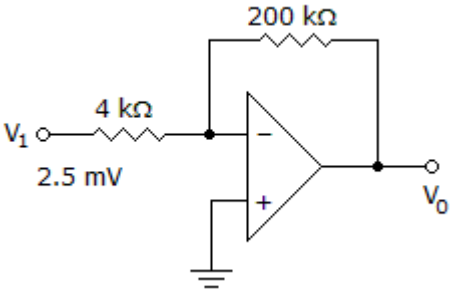
B. 4.65 V

C. 6.45 V

D. –6.45 V

Answer: Option D

43. Determine the output voltage for this circuit with a sinusoidal input of 2.5 mV.



A. –0.25 V

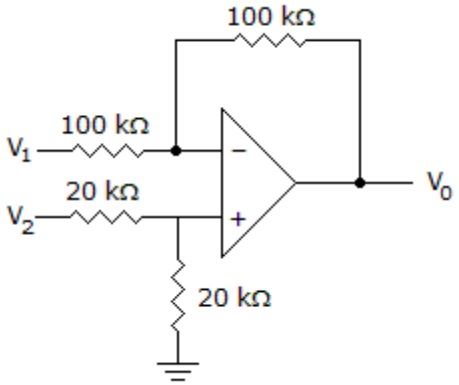
B. –0.125 V

C. 0.25 V

D. 0.125 V

Answer: Option B

44. Determine the output voltage when $V_1 = V_2 = 1$ V.



A. 0 V

B. –2 V

C. 1 V

D. 2 V

Answer: Option A

45. How many op-amps are required to implement this equation?

$$V_o = -\left(\frac{R_f}{R_2} V_2 - \frac{R_f}{R_3}\frac{R_f}{R_1} V_1\right)$$

A. 2

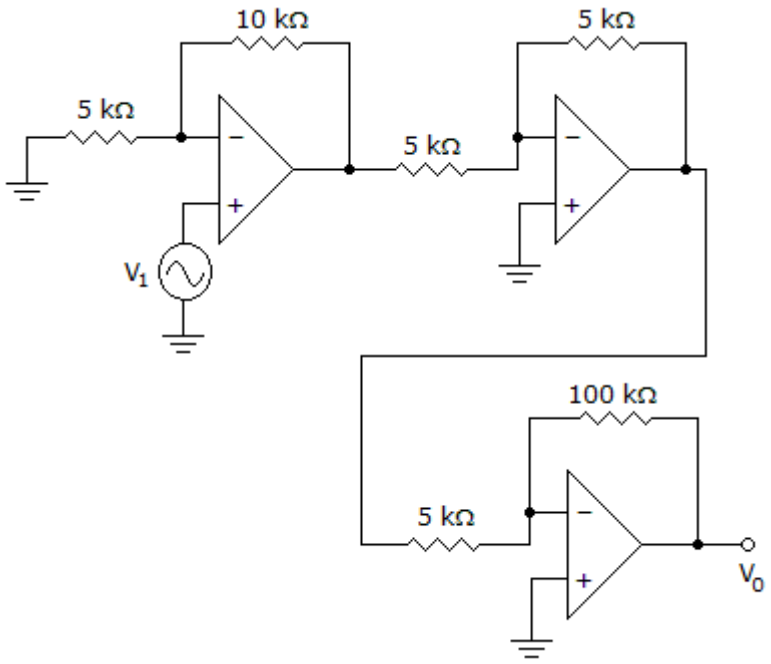
B. 3

C. 4

D. 1

Answer: Option A

46. Calculate the input voltage if the final output is 10.08 V.



A. –1.05 V

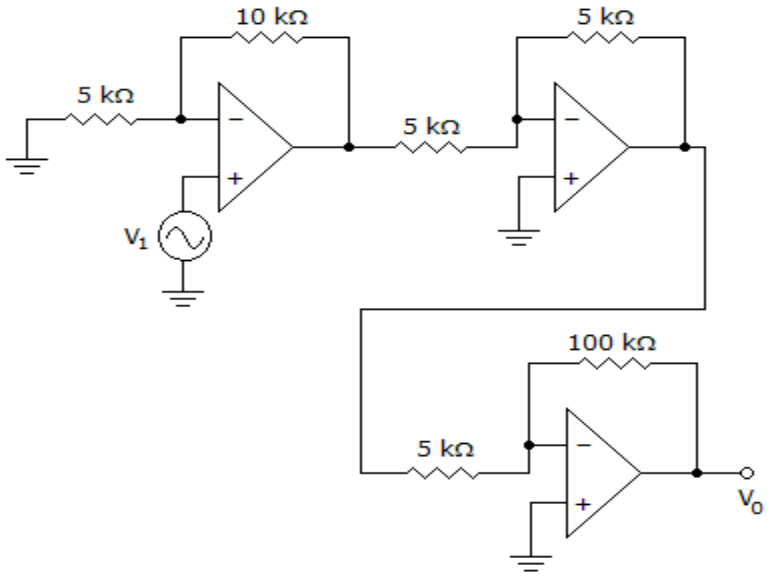
B. 0.525 V

C. 0.168 V

D. 4.2 V

Answer: Option C

47. Calculate the output of the first-stage op-amp when V_1 = 25 mV



A. –1.05 V

B. 0.075 V

C. 0.06 V

D. 4.2 V

Answer: Option B

48. How many op-amps are required to implement this equation?

$$V_o = \frac{R_3}{R_1 + R_3} \frac{R_2 + R_4}{R_2} V_1 - \frac{R_4}{R_2} V_2$$

A. 2

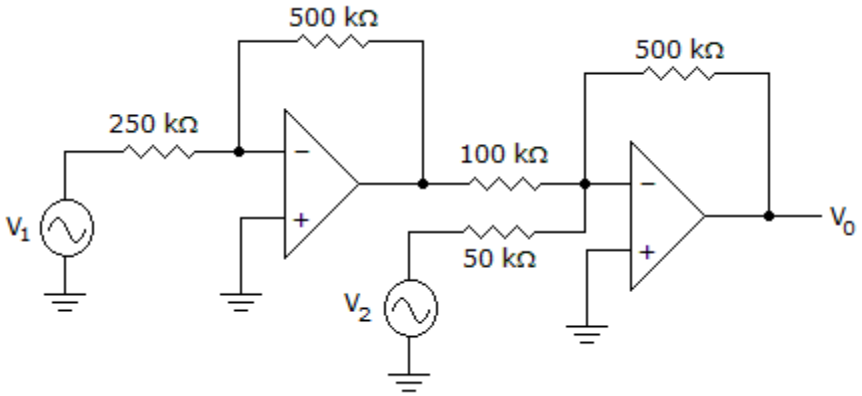
B. 3

C. 4

D. 1

Answer: Option D

49. Calculate the output voltage if $V_1 = V_2 = 700$ mV.



A. 0 V

B. –12 V

C. 12 V

D. –8 V

Answer: Option A

50. Calculate the cutoff frequencies of a bandpass filter with R1 = R2 = 5 k and C1 = C2 = 0.1 F.

A. fOL = 318.3 Hz, fOH = 318.3 Hz

B. fOL = 636.6 Hz, fOH = 636.6 Hz

C. fOL = 318.3 Hz, fOH = 636.6 Hz

D. fOL = 636.6 Hz, fOH = 318.3 Hz

Answer: Option A

51. Calculate the output voltage if V1 = 300 mV and V2 = 700 mV.

A. 0 V

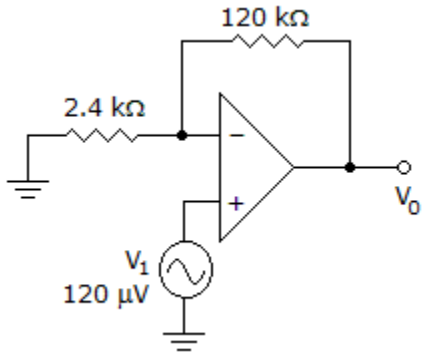
B. –12 V

C. 12 V

D. –4 V

Answer: Option D

52. Calculate the output voltage.



A. –6.00 mV

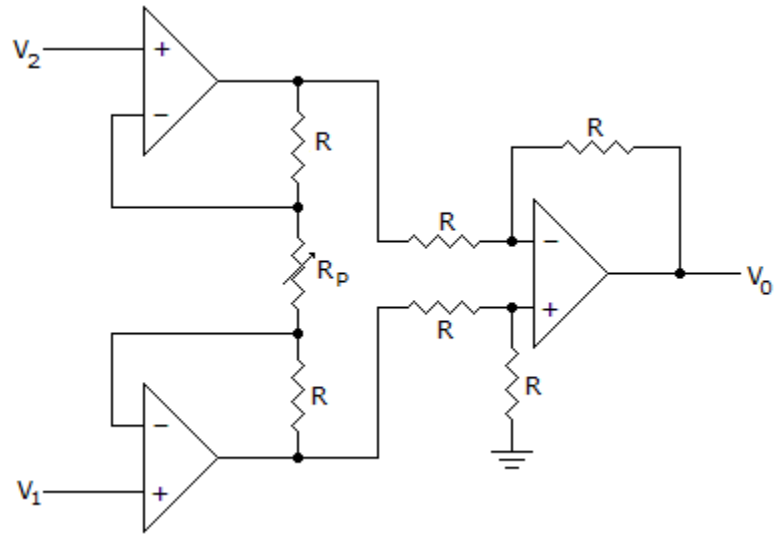
B. 6.0 mV

C. 6.12 mV

D. –6.12 mV

Answer: Option C

53. This circuit is an example of a(n)_____.



A. dc voltmeter

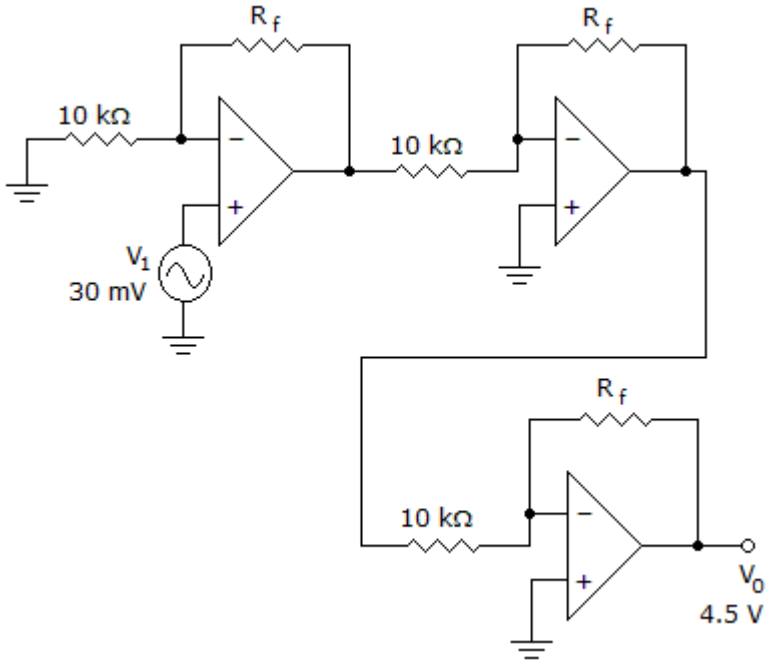
B. display driver

C. instrumentation amplifier

D. None of the above

Answer: Option C

54. Determine the value of Rf (assuming that all have the same value).



A. 500 k

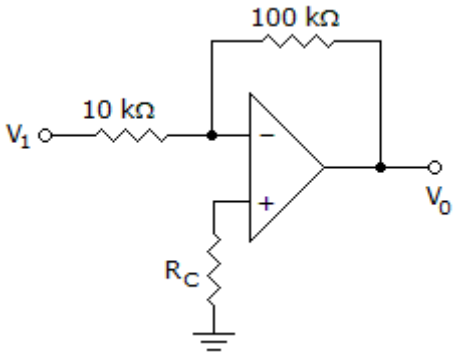
B. 50 k

C. 25 k

D. 5 k

Answer: Option B

55. Calculate the input voltage for this circuit if V_o = –11 V.



A. 1.1 V

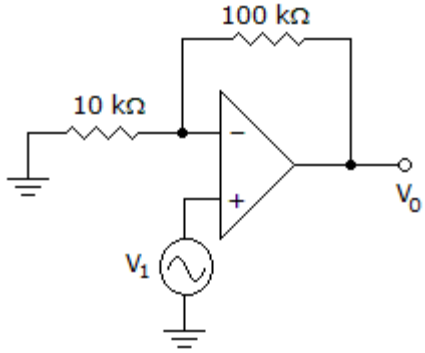
B. –1.1 V

C. –1 V

D. 1 V

Answer: Option A

56. Calculate the input voltage when V_o = 11 V.



A. 1.1 V

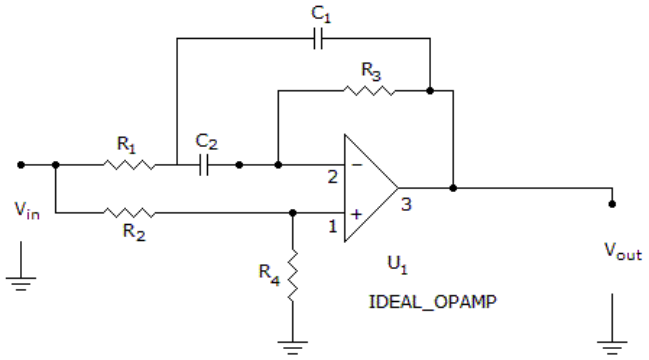
B. –1.1 V

C. –1 V

D. 1 V

Answer: Option D

57. What is this circuit?



[A]. a low-pass filter

[B]. a high-pass filter

[C]. a bandpass filter

[D]. a band-stop filter

Answer: Option D

QB2:

EE AND ECE IMPORTANT MCQ PDF-Integrated Circuits & Hybrid Parameters

1 Integrated Circuits

Q1. An IC has …….. size

1. Very large
2. Large
3. Extremely small
4. None of the above

Answer : 3

Q2. ICs are generally made of ……

1. Silicon
2. Germanium
3. Copper
4. None of the above

Answer : 1

Q3. …… ICs are the most commonly used

1. Thin films
2. Monolithic
3. Hybrid
4. None of the above

Answer : 2

Q4. The most popular form of IC package is ……..

1. DIL
2. Flatpack
3. TO-5
4. None of the above

Answer : 2

Q5. ……. cannot be fabricated on an IC

1. Transistors
2. Diodes
3. Resistors
4. Large inductors and transformers

Answer : 4

Q6. An audio amplifier is an example of ……

1. Digital IC
2. Linear IC
3. Both digital and linear IC
4. None of the above

Answer : 2

Q7. The active components in an IC are …….

1. Resistors
2. Capacitors
3. Transistors and diodes
4. None of the above

Answer : 3

Q8. We use …….. ICs in computers

1. Digital
2. Linear
3. Both digital and linear
4. None of the above

Answer : 1

Q9. The SiO2 layer in an IC acts as …….

1. A resistor
2. An insulating layer
3. Mechanical output
4. None of the above

Answer : 2

Q10. ICs are used in ……

1. Linear devices only
2. Digital devices only
3. Both linear and digital devices
4. None of the above

Answer : 3

Q11. A transistor takes …… inductor on a silicon IC chip

1. Less space than
2. More space than

3. Same space as
4. None of the above

Answer : 1

Q12. The most popular types of ICs are ……..

1. Thin-film
2. Hybrid
3. Thick-film
4. Monolithic

Answer : 4

Q13. Digital ICs process …….

1. Linear signals only
2. Digital signals only
3. Both digital and linear signals
4. None of the above

Answer : 3

Q14. Operational amplifiers use ……..

1. Linear ICs
2. Digital ICs
3. Both linear and digital ICs
4. None of the above

Answer : 2

Q15. Which of the following is most difficult to fabricate in an IC?

1. Diode
2. Transistor
3. FET
4. Capacitor

Answer : 4

Hybrid Parameters

Q1. Hybrid means ……

1. Mixed
2. Single
3. Unique

4. None of the above

Answer : 1

Q2. There are …… *h* parameters of a transistor

1. Two
2. Four
3. Three
4. None of the above

Answer: 2

Q3. The *h* parameter approach gives correct results for ……

1. Large signals only
2. Small signals only
3. Both small and large signals
4. None of the above

Answer: 2

Q4. A transistor behaves as a linear device for …….

1. Small signals only
2. Large signals only
3. Both small and large signals
4. None of the above

Answer : 1

Q5. The parameter h_{ie} stands for input impedance in ……..

1. CB arrangement with output shorted
2. CC arrangement with output shorted
3. CE arrangement with output shorted
4. None of the above

Answer : 3

Q6. The dimensions of h_{ie} parameter are ……..

1. Mho
2. Ohm
3. Farad
4. None of the above

Answer : 2

Q7. The h_{fe} parameter is called ……. in CE arrangement with output shorted

1. Voltage gain
2. Current gain
3. Input impedance
4. None of the above

Answer : 2

Q8. If the operating point changes, the *h* parameters of transistor ……..

1. Also change
2. Do not change
3. May or may not change
4. None of the above

Answer : 1

Q9. The values of *h* parameter of a transistor in CE arrangement are …… arrangement

1. The same as for CB
2. The same as for CC
3. Different from that in CB
4. None of the above

Answer : 3

Q10. In order to determine h_{fe} and h_{ie} parameters of a transistor, …… is an a.c. short circuited

1. Input
2. Output
3. Input as well as output
4. None of the above

Answer : 2

Q11. If temperature changes, *h* parameters of a transistor ……

1. May or may not change
2. Do not change
3. Also change
4. None of the above

Answer : 3

Q12. In CE arrangement, the value of input impedance is approximately equal to ……..

1. H_{ie}
2. H_{oe}
3. H_{re}
4. None of the above

Answer : 1